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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/562,945	12/28/2005	Lechong Chen	42P18502	6166

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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

EXAMINER	
TRUONG, LECHI	
ART UNIT	**PAPER NUMBER**
2194	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/562,945	CHEN ET AL.	
	Examiner	Art Unit	
	LeChi Truong	2194	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/ are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

WILLIAM THOMSON
SUPERVISORY PATENT EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-27 are presented for the examination.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3, 4, 7-10, 12-14, 16-18, 22-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chintalapati et la (US. 6, 988,140 B2) in view of Park et al(US. Patent 6,711643 B2) and further in view of Jack (6584560).

As to claim 1, Chintalalpati teaches the invention substantially as claimed including: the first processor (server process 210, col 7, ln 30-35/ a processor 504, col 15, ln 15-20/ Fig. 2), a timer interrupt process(how long each connection is idle and close connections that have been idle for a predetermined time period, col 5, ln 10-16), the first processor to handle a polling function for a timer interrupt process(col 7, ln 30-45), a normal execution thread to be processed by the second process(processing resource, col 5, ln 9-12/ processing resources ... manly worker threads 240, 141, 144, col 6, ln 30-40/ ln 63-67), setting a timer for a plurality of time intervals (a predetermined time interval has elapsed, X seconds, col 8, ln 43-45), calling a polling function

(the polling system call, col 8, ln 46-50/ col 12, ln 32-35/ln 42-50/ ln 55-57), a polling function (a poll request, col 8,ln 39-45), a polling function at the end of each of the plurality of time intervals (col 8, ln 39-45), any special vents (the type of event, such as a data request or an exception that indicates that client has closed the connection, col 7, ln 53-58) the polling unction to determine if any special events have occurred(col 7, ln 50-58) the polling function being performed by a first processor(col 20, ln 7-10), a positive result(active, col 5, ln 10/ col 8, ln 1-7) , if the polling function results in a positive result, processing the results of the polling function with a second processing(col 5, ln 1-10, col 8, ln 1-7).

Chintalapati does not explicitly teach the the second process as the second processor. However, Park teaches the second processor (The master processor 300 [first processors] reads the status register [poll] of the vectored interrupt controller 400 and analyzes the source of the interrupt so as to process the interrupt received through the IRQ signal. If the interrupt is requested by a functioning unit controlled by the first ARM processor 100 designated as the slave processor according to the analyzed results, the master processor 300 sends both an interrupt redirection request and content of corresponding interrupt to the interrupt redirection unit 200 using the internal bus 900. The interrupt redirection unit 200 requests an interrupt by activating an FIQ signal connected to the slave processor 100 according to the received interrupt redirection request. After receiving the interrupt through the FIQ signal, the slave processor 100[the second processor] accesses the interrupt redirection unit 200 through the internal bus 900, confirms the contents of the corresponding interrupt and processes the interrupt, col 5, ln 41-57).

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the teaching of Chintalapati with Park to incorporate the feature of the

second processor because this utilizes the inter-processor communication exclusive bus for connecting between exclusive controllers.

Chintalapati and Park do not teach initializing a computer system including a fist processor and a second processor. However, Jack teaches initializing a computer system including a fist processor and a second processor(identifying at least one of the plurality of computer processors, the initialization control circuit operable to assert signals on the bus request lines such that the at least one computer processor identified in the memory initializes the computer system, col 6, ln 15-20).

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the teaching of Chintalapati and Park with Jack to incorporate the feature of initializing a computer system including a fist processor and a second processor because this achieves greater efficiency by assigning each component of such a task to a different processor so that they can be performed in parallel.

As to claim 3, Chintalapati teaches the first processor is an application processor (col 15, ln 50-51).

As to claim 4, Chintalapati teachers declaring the first processor to be dedicated to the polling function (col 20, ln 7-9).

As to claim 7, Chintalapati teaches asynchronous event handling for the first processor and the second processor (col 4, ln 29-33).

As to claim 8, it is an apparatus claim of claim 1; therefore, it is rejected for the same reason as claim 1 above. In additional, Chintalapati teaches the first processor designated to handle a timer interrupt process (col 7, ln 30-40).

As to claim 9, Chintalapati teaches the performance of the polling operation overlaps at least in part with the performance of the normal processing operation (col 5, ln 3-10).

As to claim 10, Chintalapati teaches the first processor is dedicated to event handling (col 7, ln 55-58).

As to claim 12, Sugahara teaches the first processor and the second processor is separate physical processors (col 2, ln 7-10).

As to claim 13, Sugahara teaches the first processor and the second processor are logical processors in a single physical processor (Fig. 2).

As to claim 14, it is an apparatus claim of claim 1; therefore, it is rejected for the same reason as claim 1 above. In additional, Chintalapati teaches event (col 4, ln 62-67), the event handling function of the first processor, polling of events (col 7, ln 50-58),

As to claims 16, 17, they are apparatus claims of claims 3, 6; therefore, they are rejected for the same reasons as claims 3, 6 above.

As to claim 18, Chintalapati teaches event mechanism for the computer system (col 8, ln 38-45).

As to claims 22, 24-27, they are apparatus claims of claims 1, 3, 4, and 9; therefore, they are rejected for the same reasons as claims 1, 3, 4, and 9 above.

As to claim 23, Chintalapati teaches the polling function comprises polling a computer interface (col 8, ln 1-3).

3. Claims 2, 11 rejected under 35 U.S.C. 103(a) as being unpatentable over Chintalapati et la (US. 6, 988,140 B2) in view of Park et al (US. Patent 6,711643 B2) in view of Jack (6584560), as applied to claim 1 above, and further in view of Hoa (US. Patent 7296069).

As to claim 2, Chintalapati, Park and Jack do not teach a network stack, polling a network interface card. However, Hoa teaches a network stack, polling a network interface card(a protocol stack, col 9, ln 30-35/ wherein the polling interval is configurable by users; querying the status of each network interface card, col 9, ln 45-55).

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the teaching of Chintalapatim Park and Jack with Hoa to incorporate the feature of a network stack, polling a network interface card because this minimizes communications errors and establishes point to point connections between two host computers.

As to claim 11, it is an apparatus claim of claim 2; therefore, it is rejected for the same reason as claim 2 above.

5. Claims 5, 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Chintalapati ET la (US. 6, 988,140 B2) in view of Park et al (US. Patent 6,711643 B2) in view of Jack (6584560), as applied to claim 1 above, and further in view Karnik et al (US. 5,724527).

As to claim 5, Chintalapati, Park and Jack do not teach bootstrap processor. However, Morris teaches bootstrap processor (the bootstrap processor, col 3, ln 1-3).

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the teaching of Chintalapati, Park and Jack with Karnik to incorporate the feature bootstrap processor because this allows different processors to be dedicated to perform predetermined functions or tasks faster and more efficiently.

As to claim 15, it is an apparatus claim of claim 5; therefore, it is rejected for the same reason as claim 5 above.

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chintalapati et la (US. 6, 988,140 B2) in view of Park et al (US. Patent 6,711643 B2) in view of Jack (6584560), as applied to claim 1 above, and further in view Yamanoto (Facsimile equipment).

As to claim 6, Chintalapati teaches a normal execution thread (col 8, ln 1-6).

Chintalapati and Sugahara do not processing in parallel with polling function. Yamanoto teaches processing in parallel with polling function (a polling setting memory 11b for storing a multipolling reception stard data and time and a group number and a signal processing, Sec: Constitution, ln 4-7/ executing the input processing of the succeeding multipolling start data and time and the group number in parallel with polling reception processing, page 2, ln 1-4).

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the teaching of Chintalapati and Sugahara to incorporate the feature of processing in parallel with polling function because this provides a possibility to set up the reservation of the succeeding multipolling immediately after the start of multipolling.

5. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chintalapati et la (US. 6, 988,140 B2) in view of Park et al (US. Patent 6,711643 B2) in view of Jack (6584560), as applied to claim 1 above, and further in view of Yang et al (US. Patent 7,003610 B2).

As to claim 19, Chintalapati, Park and Jack do not explicitly teach a single thread. However, Yang teache a single thread (single thread, col 3, ln 37-40).

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the teaching of Chintalapati, Park and Jack with Yang to incorporate the feature of a single thread because this provides the servicing for all write requests received via interrupts in a single thread with limited memory space and avoids shared resource conflicts.

6. Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chintalapati et la (US. 6, 988,140 B2) in view of Park et al (US. Patent 6,711643 B2) in view of Jack (6584560), as applied to claim 1 above, and further in view of Hokenek et al (US 6,971, 103 B2).

As to claim 20, Chintalapati, Park and Jack do not teach a multi-processor system. However, Hokenek teaches multi-processor (Multi-proccessor, col 1, ln 30-33).

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the teaching of Chintalapati, Park and Jack with Hokenek to incorporate the feature of a multi-processor because this provides a low-latency, low-everhead mechanism for delivering and servicing cross thread interrupts in a multithreaded processors.

As to claim 21, Hokenek teaches a hyper-threaded system (col 1, ln 63-67).

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LeChi Truong whose telephone number is (571) 272 3767. The examiner can normally be reached on 8 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomson, William can be reached on (571) 272 3718. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR of Public PAIP. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIP system, contact the Electronic Business Center (EBC) at 866-217-9197(toll-free).

LeChi Truong

January 3, 2008

WILLIAM THOMSON
SUPERVISORY PATENT EXAMINER